

3L Diamond application note

Using Xilinx Chipscope in a Diamond project

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Related documents

Acronyms, Abbreviations and Definitions

Overview

Xilinx Chipscope allows observing the internal state of the FPGA while it is loaded with a bitstream. This application note explains how to use Xilinx Chipscope in a Diamond FPGA application.

The host PC should be connected to the FPGA via a JTAG cable and Xilinx Chipscope should be installed.

Inserting Xilinx Chipscope in the VHDL file of a task

When using this method you will insert Xilinx Chipscope component in the source files of the task that you wish to debug.

Generate the Xilinx Chipscope components

The first step is to generate the Xilinx Chipscope components ILA and ICON that you wish to use. To do so launch Xilinx Chipscope Generator and customize the component with the feature you'd like to have.

Add the Xilinx Chipscope files to your task

Then, you need to add the files representing the Xilinx Chipscope component to your Diamond task.

The following files should be added:

- Icon.edn
- Icon.ncf
- Ila.edn
- Ila.ncf

Instantiate Xilinx Chipscope in your VHDL

Instantiate the Xilinx Chipscope components in the VHDL of your task and connect them accordingly.

The following VHDL snippet is an example.

Architecture rtl of mytask is

```
component icon
  port
  (
    control0      :   out std_logic_vector(35 downto 0)
  );
end component;

component ila
  port
  (
    control      : in   std_logic_vector(35 downto 0);
    clk          : in   std_logic;
  );
end component;
```

```
        data      : in    std_logic_vector(15 downto 0);
        trig0     : in    std_logic_vector(7  downto 0)
    );
end component;

    signal control: std_logic_vector(35 downto 0);

Begin

i_icon: icon
port map (control);

i_ila: ila
port map (control, clk, data, trig0);

data <= "the signals that you want to observe"
trig0 <= "the signals that you want to use to trigger Xilinx Chipscope"

End;
```

Inserting Xilinx Chipscope the netlist of the design

This feature is not currently supported.

Debug the application

Build and run the application.

Once the FPGA is configured start Xilinx Chipscope Analyser and connect to the target. You should then be able to use Xilinx Chipscope to observe the signals inside the FPGA.

Revision history